WE CLAIM:

1. A feedback latch circuit comprising:

a first logic OR gate having a clock input terminal for receiving a clock input signal, a data input terminal, and an output terminal;

a first logic AND gate having a first data input terminal coupled to said output terminal of said first logic OR gate, a second data input terminal for receiving a data input signal, and an output terminal;

a second logic AND gate having a data input terminal coupled to said data input terminal of said first logic OR gate, a clock input terminal for receiving a complementary clock input signal that complements the clock input signal, and an output terminal; and

a second logic OR gate having a first data input terminal coupled to said output terminal of said first logic AND gate, a second data input terminal coupled to said output terminal of said second logic AND gate, and an output terminal coupled to said data input terminals of said first logic OR gate and said second logic AND gate;

wherein a latch output of said feedback latch circuit is obtained from said output terminal of said second logic OR gate.

2. A latch-incorporating circuit comprising:

a set of first logic OR gates, each of which has a clock input terminal for receiving a clock input signal,

a data input terminal, and an output terminal;

a set of first logic AND gates, each of which has a first data input terminal coupled to said output terminal of a respective one of said first logic OR gates, a number of data input terminals, each of which receives a data input signal, and an output terminal;

a second logic AND gate having a data input terminal coupled to said data input terminal of each of said first logic OR gates, a clock input terminal for receiving a complementary clock input signal that complements the clock input signal, and an output terminal; and

a second logic OR gate having a set of first data input terminals coupled respectively to said output terminals of said first logic AND gates, a second data input terminal coupled to said output terminal of said second logic AND gate, and an output terminal coupled to said data input terminals of said first logic OR gates and said second logic AND gate;

wherein a data output signal of said latch-incorporating circuit is obtained from said output terminal of said second logic OR gate.

3. A latch-incorporating circuit comprising:

a first logic OR gate having a clock input terminal for receiving a clock input signal, a data input terminal, and an output terminal;

a set of first logic AND gates, each of which has a first data input terminal coupled to said output

terminal of said first logic OR gate, a number of data input terminals, each of which receives a data input signal, and an output terminal;

a second logic AND gate having a data input terminal coupled to said data input terminal of said first logic OR gate, a clock input terminal for receiving a complementary clock input signal that complements the clock input signal, and an output terminal; and

a second logic OR gate having a set of first data input terminals coupled respectively to said output terminals of said first logic AND gates, a second data input terminal coupled to said output terminal of said second logic AND gate, and an output terminal coupled to said data input terminals of said first logic OR gate and said second logic AND gate;

wherein a data output signal of said latch-incorporating circuit is obtained from said output terminal of said second logic OR gate.

4. A feedback latch circuit comprising:

a first logic OR gate for performing a logic OR operation upon a clock input signal and a latch output;

a first logic AND gate, coupled to said first logic OR gate, for performing a logic AND operation upon output of said first logic OR gate and a data input signal;

a second logic AND gate for performing a logic AND operation upon a complementary clock input signal and the latch output, the complementary clock input signal

complementing the clock input signal; and

a second logic OR gate, coupled to said first logic OR gate and said first and second logic AND gates, for performing a logic OR operation upon outputs of said first and second logic AND gates to result in the latch output that is provided to said first logic OR gate and said second logic AND gate.

5. A latch method comprising:

performing a logic OR operation upon a clock input signal and a latch output to obtain a first logic OR output;

performing a logic AND operation upon the first logic OR output and a data input signal to obtain a first logic AND output;

performing a logic AND operation upon a complementary clock input signal and the latch output to obtain a second logic AND output, the complementary clock input signal complementing the clock input signal; and

performing a logic OR operation upon the first and second logic AND outputs to result in the latch output.